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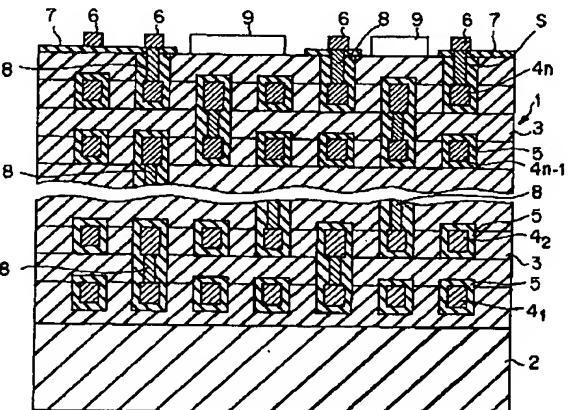
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(54)【発明の名称】 回路基板

(57)【要約】

【目的】 配線部の信号伝搬速度を高めると共に、高熱伝導性を有する回路基板を提供しようとするものである。

【構成】 窒化アルミニウム、窒化硼素、炭化硼素、ダイヤモンドライカーボンおよびダイヤモンドから選ばれた少なくとも1種からなる高熱伝導性材料からなる絶縁層3と、前記絶縁層3に埋め込まれた配線部4₁、4₂…4_{n-1}と、前記配線部4₁、4₂…4_{n-1}の周囲に形成された非晶質窒化アルミニウム、非晶質酸化珪素、酸化珪素および硼珪酸ガラスから選ばれた少なくとも1種の低誘電率材料からなる誘電体膜5とを具備したことを特徴としている。



【特許請求の範囲】

【請求項1】 窒化アルミニウム、窒化硼素、炭化硼素、ダイヤモンドライクカーボンおよびダイヤモンドから選ばれた少なくとも1種の高熱伝導性材料からなる絶縁層と、前記絶縁層に埋め込まれた配線部と、前記配線部の周囲に形成された非晶質窒化アルミニウム、非晶質酸化珪素、酸化珪素および硼珪酸ガラスから選ばれた少なくとも1種の低誘電率材料からなる誘電体膜とを具備したことを特徴とする回路基板。

【発明の詳細な説明】

【0001】

【産業上の利用分野】 本発明は、半導体チップ等が搭載される回路基板に関する。

【0002】

【従来の技術】 コンピュータシステムの高速化、小形化指向は前記システムに使用する半導体チップの高速化、高集積化をより加速し、最近ではクロック周波数が100MHz、チップ当たりの消費電力が30W以上のものが使用されつつある。

【0003】 ところで、前記半導体チップが搭載される回路基板としては従来より高熱伝導性の窒化アルミニウムからなる誘電体材料で配線部間を絶縁する絶縁層を形成した構造のものが知られている。しかしながら、前記回路基板は半導体チップにおける高放熱化に対応できるものの、前記窒化アルミニウムからなる誘電体材料の誘電率が比較的高いために配線部の信号伝搬速度を遅延させ、高速化に対応できないという問題があった。

【0004】 このようなことから、高熱伝導性材料からなる基材上に例えば酸化珪素などの低誘電率材料からなる絶縁層を薄膜プロセスで形成し、前記絶縁層の間に配線部を埋め込んだ構造の回路基板が提案されている。しかしながら、前記回路基板に半導体チップを搭載した場合、前記半導体チップと前記高熱伝導性材料からなる基材の間に熱伝導性の低い酸化珪素等の低誘電率材料からなる絶縁層が介在されているため、放熱性が不十分で、前記配線部の信号伝搬速度の向上のみしか達成することができなかった。

【0005】

【発明が解決しようとする課題】 上述したように従来の回路基板においては、半導体チップ等の高速化、高集積化に対応して信号伝搬速度と放熱性を同時に向上させることは困難であり、高速動作性および高放熱性を兼ね備えた回路基板の開発が要望されていた。

【0006】 本発明は、前記要望に答え、配線部の信号伝搬速度を高めると共に、高熱伝導性を有する回路基板を提供しようとするものである。

【0007】

【課題を解決するための手段】 本発明に係わる回路基板は、窒化アルミニウム、窒化硼素、炭化硼素、ダイヤモンドライクカーボンから選ばれた少なくとも1種の高熱

伝導性材料からなる絶縁層と、前記絶縁層に埋め込まれた配線部と、前記配線部の周囲に形成された非晶質窒化アルミニウム、非晶質窒化珪素、酸化珪素および硼珪酸ガラスから選ばれた少なくとも1種の低誘電率材料からなる誘電体膜とを具備したことを特徴とするものである。

【0008】 次に、本発明に係わる回路基板の断面図を図1、その一部を拡大した断面図を図2に示して以下に詳細に説明する。

【0009】 回路基板1は、窒化アルミニウム、窒化硼素、炭化硼素、ダイヤモンドライクカーボンおよびダイヤモンドから選ばれた少なくとも1種の高熱伝導性材料からなる基材2を備えている。前記高熱伝導性材料からなる絶縁層3は、前記基材2上に複数積層されている。配線部となる内部配線層4₁、4₂…4_{n-1}、4_nは、前記絶縁層3内に通常、複数層形成されている。非晶質窒化アルミニウム、非晶質酸化珪素、酸化珪素および硼珪酸ガラスから選ばれた少なくとも1種の低誘電率材料からなる誘電体膜5は、前記内部配線層4₁、4₂…4_{n-1}、4_nの周囲に形成されている。表面配線層6は、前記絶縁層3上に前記低誘電率材料からなる誘電体膜7を介して形成されている。スルホール8は、前記内部配線層4₁、4₂…4_{n-1}、4_nおよび前記表面配線層6とのうち所望の配線層間を接続するために形成されている。なお、前記絶縁層3上の前記誘電体膜7は、一部が除去されて前記絶縁層3表面が露出され、このような露出面に例えば半導体チップ9が搭載される。

【0010】 前記内部配線層4₁、4₂…4_{n-1}、4_n間に位置する前記絶縁層3の厚さ、すなわち図2中のt₁は、次のような理由により0.5～15μmの範囲にすることが望ましい。すなわち、前記絶縁層3の厚さ(t₁)を0.5μm未満にすると前記内部配線層4₁、4₂…4_{n-1}、4_n間を十分に電気的に分離することが困難になる。一方、前記絶縁層3の厚さ(t₁)が15μmを超えるとその内部応力によって下地(例えば前記基材1)から剥離する恐れがある。より好ましい前記絶縁層3の厚さ(t₁)は、0.9～10μmである。

【0011】 前記内部配線層4₁、4₂…4_{n-1}、4_nを包囲する前記誘電体膜5の厚さ、すなわち図2中のt₂は、次のような理由により0.4～15μmの範囲にすることが望ましい。すなわち、前記誘電体膜5の厚さ(t₂)を0.4μm未満にすると前記内部配線層4₁、4₂…4_{n-1}、4_nを確実に覆うことが困難になり、信号伝搬速度を高めることが困難になる。一方、前記誘電体膜5の厚さ(t₂)が15μmを超えると前記誘電体膜5の内部応力が大きくなつて前記絶縁層3から剥離する恐れがある。

【0012】 前記内部配線層4₁、4₂…4_{n-1}、4_nおよび表面配線層6は、例えばAlやTi/Cuまたは

Ti/Ni/Au等の多層構造のもの等を用いることができる。

【0013】前記表面配線層6は、前記絶縁層3上に低誘電率材料からなる誘電体膜7を介して形成することが望ましいが、前記表面配線層6の引き回し長さが短い場合には前記高熱伝導性材料からなる前記絶縁層3上に直接形成してもよい。

【0014】なお、図1で示した回路基板ではスルホール8が低誘電率材料からなる誘電体膜7で包囲されているが、スルホール8の長さが短い場合は、スルホール8が誘電体膜7で特に包囲されなくともよく、配線部である内部配線層4₁、4₂…4_{n-1}、4_nの周囲のみに誘電体膜7を形成することができる。

【0015】さらに、本発明に係わる回路基板は絶縁層3中に埋め込まれる配線層は単層であってもよい。

【0016】次に、本発明に係わる回路基板の製造方法を図3～図6を参照して詳細に説明する。

【0017】まず、図3(A)に示すように前述した高熱伝導性材料からなる基材11上に同様な高熱伝導性材料からなる絶縁層12をスパッタ法、CVD法、イオンプレーティング法、クラスタイオンビーム法等の薄膜形成法により堆積する。なお、前記絶縁層12の形成に先立って湿式洗浄法、逆スパッタ法などで前記基材11表面を清浄化してもよい。つづいて、図3(B)に示すように前記絶縁層12をフォトエッチング技術により選択的に除去して形成すべき内部配線層とほぼ同じ長さで所望の幅、深さを有する複数の溝部13を形成した後、前記薄膜形成法により前述した低誘電率材料を堆積し、さらに前記絶縁層12上の誘電体膜を除去することにより前記溝部13内に誘電体14を埋め込む。ひきつづき、前記誘電体膜1をフォトエッチング技術により選択的に除去して図3(C)に示すように形成すべき内部配線層と同じ長さ、幅、深さを有する断面凹状の誘電体膜15を形成する。

【0018】次いで、A1などの配線材料を前記薄膜形成法により全面に堆積し、前記絶縁層12表面の配線材料膜を除去することにより前記断面凹状の各誘電体膜15内に第1層の内部配線層16₁を埋め込む。つづいて、前述した低誘電率材料を前記薄膜形成法により堆積し、バターニングすることにより図4(D)に示すように前記第1層の内部配線層16₁および誘電体膜15上に誘電体膜17を形成して前記内部配線層16₁の周囲を前記断面凹状の誘電体膜15および前記誘電体膜17で覆う。ひきつづき、図4(E)に示すように全面に前述した高熱伝導性材料からなる絶縁層18を前記薄膜形成法により堆積する。さらに、図4(F)に示すように前記第1層の内部配線層16₁上の所定位置の前記絶縁層18をフォトエッチング技術により選択的に除去して前記誘電体膜17まで達する複数の溝部19を形成した後、前記溝部19内に前述した低誘電率材料を前記薄膜

形成法により堆積し、前記絶縁層18上の誘電体膜を除去することにより前記溝部19に誘電体20を埋め込む。

【0019】次いで、図5(G)に示すように前記溝部19内で誘電体20をフォトエッチング技術により選択的に除去して前記内部配線層16₁の上面まで達する孔を開口した後、前記薄膜形成法により配線材料を堆積し、前記絶縁層18上の導体材料膜を除去することにより前記孔内に埋め込まれ周囲が誘電体膜21で覆われたスルホール22を形成する。つづいて、図5(H)に示すように全面に前述した高熱伝導性材料からなる絶縁層23を前記薄膜形成法により堆積し、前記絶縁層22をフォトエッチング技術により選択的に除去して前記絶縁層18表面まで達し、形成すべき内部配線層とほぼ同じ長さで所望の幅、深さを有する複数の溝部24を形成した後、前記溝部24内に前述したのと同様な方法により誘電体25を埋め込む。ひきつづき、図5(I)に示すように前記溝部24内の前記誘電体25をフォトエッチング技術により選択的に除去して形成すべき内部配線層と同じ長さ、幅、深さを有する断面凹状の誘電体膜26を形成し、さらに前記スルホール22が存在する前記誘電体25は別のマスクを用いてエッチングして前記スルホール22に達する細長状の孔を開口する。その後、前記断面凹状の誘電体膜26および前記細長スルホール22上に形成された前記孔内に配線材料を堆積することにより第2層の内部配線層16₂を埋め込む。

【0020】次いで、図6(J)に示すように前記第2層の内部配線層16₂上に前述した低誘電率材料からなる誘電体膜28を前述した手法で形成した後、全面に前述した高熱伝導性材料からなる絶縁層29を前記薄膜形成法により堆積する。つづいて、前述した図4(F)および図5(G)の工程と同様な方法により前記第2層の内部配線層16₂のうちの所定の内部配線層上に位置する前記絶縁層29をフォトエッチング技術により選択的に除去して前記誘電体膜28まで達する複数の溝部30を形成し、前記溝部30内に誘電体を埋め込み、前記誘電体をフォトエッチング技術により選択的に除去して前記第2層の内部配線層16₂の上面まで達する孔を開口した後、前記孔内に配線材料を埋め込むことにより誘電体膜31で周囲が覆われたスルホール32を形成する(図6(K)図示)。

【0021】次いで、前述した図5(H)、図5(I)、図6(J)、図6(K)の工程を繰り返して既に説明した図1に示す構造の回路基板を製造する。ただし、表面配線層の形成および前記表面配線を最上層の内部配線層と接続するためのスルホールの形成に際しては、最上層の絶縁層の上に低誘電率材料からなる誘電体膜を堆積し、溝部形成、誘電体の埋め込み、孔の開口、導体材料の前記孔内への埋め込みを行ってスルホールを形成し、さらに前記誘電体膜上に表面配線層を形成し

た後、半導体チップの搭載領域になる前記誘電体膜を選択的に除去して前記誘電体膜下の高熱伝導性材料からなる絶縁層を露出させる。

【0022】

【作用】本発明に係わる回路基板は、前述した図1に示すように窒化アルミニウム、窒化硼素、炭化硼素、ダイヤモンドライカーボンおよびダイヤモンドから選ばれた少なくとも1種の高熱伝導性材料からなる絶縁層と、前記絶縁層に埋め込まれた配線部と、前記配線部の周囲に形成された非晶質窒化アルミニウム、非晶質酸化珪素、酸化珪素および硼珪酸ガラスから選ばれた少なくとも1種の低誘電率材料からなる誘電体膜とを具備した構造になっている。このため、前記回路基板の表面にLSI等の半導体チップを搭載した場合、前記半導体チップから発生する熱を前記高熱伝導性材料からなる絶縁層により良好に放出することができる。また、前記配線部の周囲は前記低誘電率材料からなる誘電体膜で覆われているため、前記配線部の信号伝搬速度を高めることができる。したがって、高速動作性と高放熱性を兼ね備えた回路基板を提供できる。

【0023】また、前述したように薄膜プロセスにより本発明に係わる回路基板を製造することによって、前記高熱伝導性材料からなる絶縁層と低誘電率材料からなる誘電体膜を回路基板の構成部材として用いることが可能になり、さらに配線部に使用される配線材料が前記絶縁層や前記誘電体膜に拡散するのを抑制して低抵抗の配線部を実現できる。

【0024】すなわち、従来のセラミック焼結プロセスによれば、前記高熱伝導性材料からなる絶縁層と前記低誘電率材料からなる誘電体膜の焼結温度が異なる場合にはこれらを同一の回路基板内に共存させることが難しい。例えば、絶縁層として窒化アルミニウム(AIN)を、誘電体膜として硼珪酸ガラスをそれぞれ使用した場合、従来のセラミック焼結プロセスでは焼結温度がそれぞれ1700~1900°C、400~900°Cと大きく*

* 異なっている。このため、AIN焼結体からなる絶縁層と例えば硼珪酸ガラスセラミックからなる誘電体膜を交互に形成することは不可能である。また、回路基板の配線部を厚膜技術により形成する場合には、通常、絶縁層との密着強度を上げるために配線材料に無機物を始めとする各種の添加物が配合される。このため、前記回路基板に形成された配線部の抵抗率は、純金属からなるものに比べて高くなる。

【0025】これに対し、前述した薄膜プロセスは前記セラミック焼結プロセスに比べて低い温度で前記高熱伝導性材料からなる絶縁層と前記低誘電率材料からなる誘電体膜を形成することができるため、信号の高速動作性と高放熱性を兼ね備えた本発明の回路基板を製造できる。しかも、前記絶縁層および誘電体膜の材料の組み合わせの自由度も高められる。さらに、配線材料として純度が99.99%以上の金属を用いることができると共に、プロセス温度を低温(例えば480°C以下)にすることができるため、配線部に使用される配線材料が前記絶縁層や前記誘電体膜に拡散するのを抑制して低抵抗の配線部を実現できる。

【0026】

【実施例】以下、本発明の実施例を詳細に説明する。

【0027】実施例1~7

前述した図3~図6に示される回路基板を製造する工程において、絶縁層を下記表1に示す条件で形成し、誘電体膜を下記表2に示す条件で、それぞれ前記絶縁層および誘電体膜のバターニング時のエッティングを下記表3に示す条件でそれを行って前述した図1に示す回路基板を製造した。ただし、基材は前記絶縁層と同一の高熱伝導性材料をそれぞれ用いた。また、内部配線層および表面配線層に用いられる配線材料およびその膜厚を下記表3に併記した。

【0028】

【表1】

実施例	絶縁層					
	高熱伝導性材料	成膜方法	基材温度(°C)	真空度(Pa)	成膜速度(nm/min)	厚さ(μm)
1	AIN	スパッタ	100	0.5	20	9
2	AIN	スパッタ	50	1	15	10
3	SiC	CVD	400	50	600	5
4	BN	CVD	250	20	50	3
5	ダイヤモンドライカーボン	CVD	150	50	100	10
6	ダイヤモンド	CVD	300	100	100	5
7	AIN	CVD	480	50	100	3

【0029】

* * 【表2】

実施例	誘電体膜					
	低誘電率材料	成膜方法	基材温度 (°C)	真 空 度 (Pa)	成膜速度 (nm/min)	厚 さ (μm)
1	硼珪酸ガラス	スパッタ	50	1	10	7
2	非晶質AlN	スパッタ	-100	0.6	105	8
3	SiO ₂	スパッタ	200	0.8	50	4
4	非晶質SiO ₂	スパッタ	-50	1.1	200	2
5	硼珪酸ガラス	スパッタ	-80	0.2	90	5
6	硼珪酸ガラス	スパッタ	-100	1	150	3
7	SiO ₂	CVD	400	200	100	1

【0030】

* * 【表3】

実施例	絶縁層／誘電体膜エッチング条件		配線	
	エッチング方法	エッチャント	材 料	膜厚 (μm)
1	湿式	HF	Al	5
2	湿式	NH ₄ OH	Ti/Ni/Au	5
3	ドライ	BCl ₃	Al	2
4	ドライ	BCl ₃	Al	1
5	湿式／ドライ	HF/O ₂	Al	3
6	湿式／ドライ	BCl ₃ /O ₂	Al	1
7	湿式／ドライ	HF/BCl ₃	Al	0.5

得られた実施例1～7の回路基板について絶縁層と誘電体膜の密着強度、内部配線層周囲の誘電率、内部配線層における単位長さ当たりの信号遅延時間および絶縁層の熱伝導率を測定した。その結果を下記表4に示す。なお、前記密着強度は前記各回路基板を2気圧、121°Cの雰

囲気に曝し、室温まで冷却する操作を1サイクルとし、1000サイクル後の状態を測定したものである。

【0031】

【表4】

実施例	回路基板の評価			
	密着強度 (MPa)	誘電率* (ε)	単位長さ当たりの信号 遅延時間 (ピコ秒/cm)	熱伝導率 (W/m·K)
1	20	6	81.6	150
2	21	6	81.6	200
3	23	3.8	64.9	110
4	25	2.8	55.7	150
5	20	1.5	40.8	2500
6	20	3	57.8	3000
7	21	4	66.6	300

誘電率* は、内部配線層周囲の値を示す。

前記表4から明らかなように、本実施例1～7の回路基板は密着強度が高く、かつ信号伝搬速度が早く、さらに高い熱伝導率を有することがわかる。したがって、本実施例1～7の回路基板に前述した図1のよう半導体チップを搭載した場合、半導体チップからの熱を良好に放散できると共に、内部配線層の信号伝搬速度が高められたために前記半導体チップを高速動作させることが可能であった。

【0032】比較例

内部配線層およびスルホールの周囲に誘電体膜を形成しなかった以外、実施例1と同様な回路基板を製造し、各特性を測定した。その結果、絶縁層の熱伝達率は150 W/m·Kと良好であったものの、内部配線層周囲の絶縁層における誘電率が9.0と大きいために信号遅延時間が99.9ピコ秒/cmと大きく、高速化への対応が困難であることが確認された。

【0033】

【発明の効果】以上詳述した如く、本発明によれば配線*

20*部の信号伝搬速度を高めると共に、高熱伝導性を有し、高速動作性と高放熱性を兼ね備えた回路基板を提供できる。

【図面の簡単な説明】

【図1】本発明の回路基板を示す断面図。

【図2】本発明の絶縁層および誘電体膜の厚さを定義するため使用した図1の部分断面図。

【図3】本発明の回路基板の製造工程を示す断面図。

【図4】本発明の回路基板の製造工程を示す断面図。

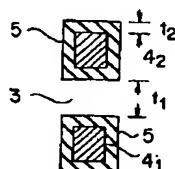
【図5】本発明の回路基板の製造工程を示す断面図。

【図6】本発明の回路基板の製造工程を示す断面図。

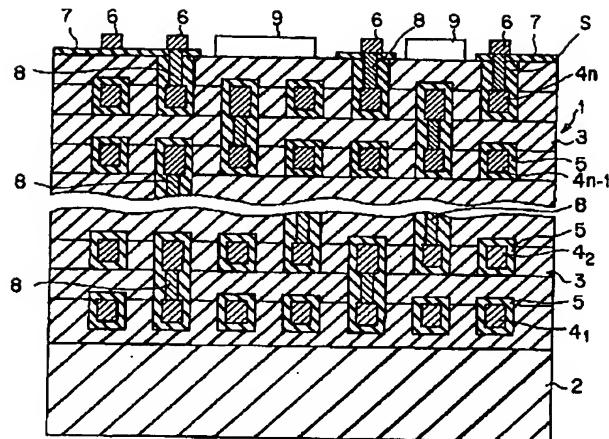
【符号の説明】

1…回路基板、2、11…基材、3、12、18、23、29…絶縁層、4₁、4₂…4_{n-1}、16₁、16₂…内部配線層、5、15、17、21、26、27、28、31…誘電体膜、8、22、32…スルホール、6…表面配線層、9…半導体チップ。

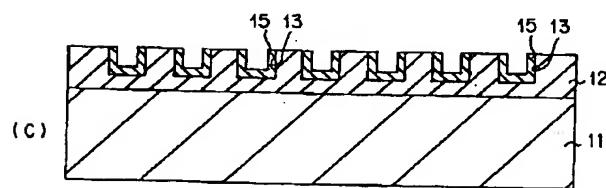
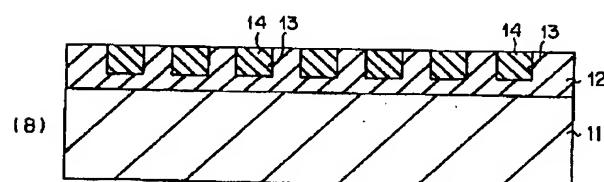
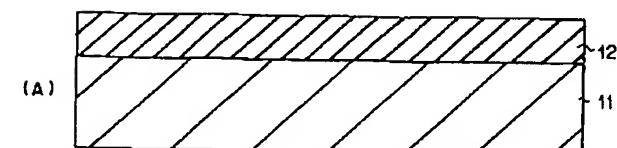
【図2】



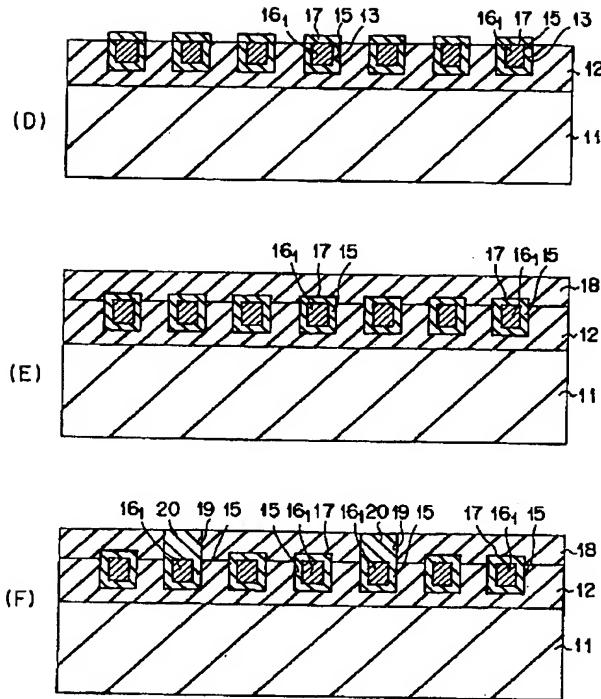
【図1】



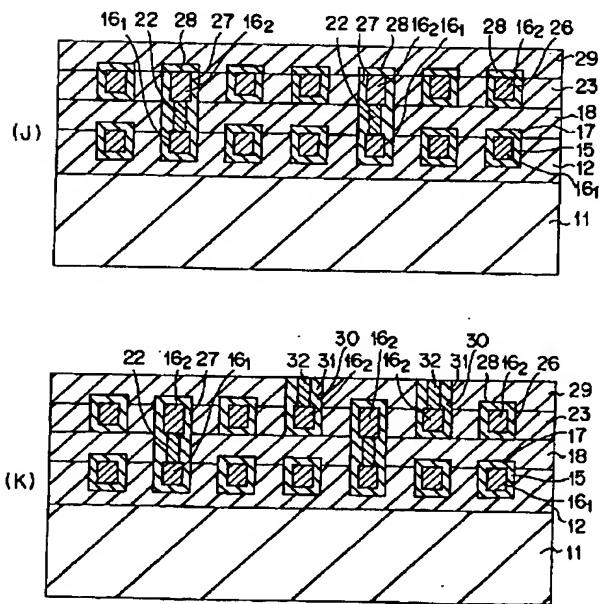
【図3】



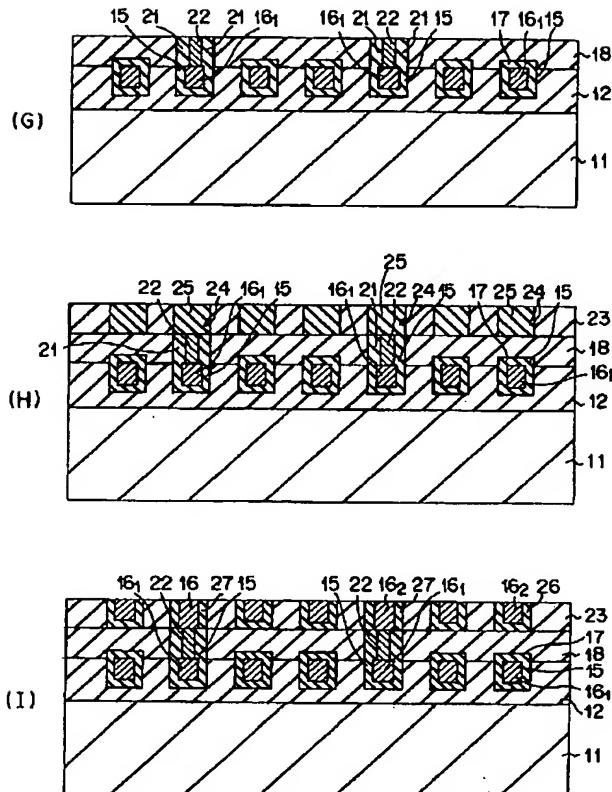
【図4】



【図6】



【図5】



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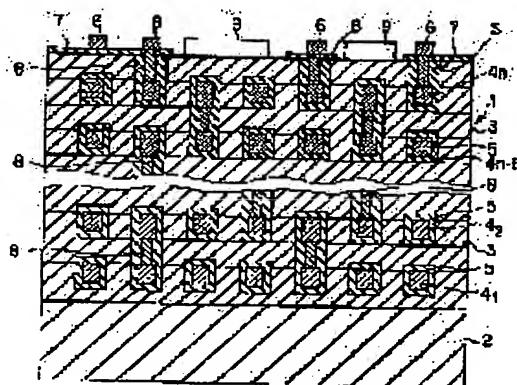
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(54) CIRCUIT BOARD

(57)Abstract:

PURPOSE: To improve the propagating speed of signals in an interconnection part and to obtain a circuit board having a high heat conductivity.

CONSTITUTION: The circuit board is provided with an insulating layer 3 consisting of a highly heat conductive material consisting of at least one kind selected from aluminum nitride, boron nitride, boron carbide, diamond-like carbon and diamond, interconnection parts 41, 42... 4n-1 buried in the insulating layer 3, and a dielectric film 5 which is formed around the interconnection parts 41, 42... 4n-1 and consists of a low-permittivity material of at least one selected from amorphous aluminum nitride, amorphous silicon oxide, silicon oxide and borosilicate glass.



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CLAIMS

[Claim(s)]

[Claim 1] The circuit board characterized by providing the dielectric film which consists of at least one sort of low dielectric constant ingredients chosen from the amorphous aluminum nitride formed in the perimeter of the insulating layer which consists of at least one sort of highly thermally-conductive materials chosen from aluminum nitride, boron nitride, boron carbide, diamond-like carbon, and a diamond, the wiring section embedded at said insulating layer, and said wiring section, amorphous oxidation silicon, oxidation silicon, and borosilicate glass.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the circuit board in which a semiconductor chip etc. is carried.

[0002]

[Description of the Prior Art] Improvement in the speed of a computer system and miniaturization orientation accelerate more improvement in the speed of the semiconductor chip used for said system, and high integration, and, recently, the thing beyond 30W is being used [a clock frequency] for 100MHz and the power consumption per chip.

[0003] By the way, the thing of the structure in which the insulating layer which insulates between the wiring sections from the former with the dielectric materials which consist of aluminium nitride of high temperature conductivity as the circuit board in which said semiconductor chip is carried was formed is known. However, although said circuit board could respond to high heat dissipation-ization in a semiconductor chip, since its dielectric constant of the dielectric materials which consist of said aluminium nitride was comparatively high, it delayed the signal velocity of propagation of the wiring section, and had the problem that it could not respond to improvement in the speed.

[0004] Since it is such, the insulating layer which consists of low dielectric constant ingredients, such as for example, oxidation silicon, is formed in a thin film process on the base material which consists of a highly thermally-conductive material, and the circuit board of the structure which embedded the wiring section between said insulating layers is proposed. However, since the insulating layer which consists of low dielectric constant ingredients, such as thermally conductive low oxidation silicon, intervened between the base materials which consist of said semiconductor chip and said highly thermally-conductive material when a semiconductor chip is carried in said circuit board, heat dissipation nature was inadequate and only improvement in the signal velocity of propagation of said wiring section was able to be attained.

[0005]

[Problem(s) to be Solved by the Invention] As mentioned above, in the conventional circuit board, it is difficult to raise signal velocity of propagation and heat dissipation nature to coincidence corresponding to improvement in the speed of a semiconductor chip etc., and high integration, and development of the circuit board which has high-speed operation nature and high heat dissipation nature was demanded.

[0006] This invention tends to offer the circuit board which has high temperature conductivity while raising the signal velocity of propagation of the wiring section responding to said request.

[0007]

[Means for Solving the Problem] The circuit board concerning this invention is characterized by providing the dielectric film which consists of at least one sort of low dielectric constant ingredients chosen from amorphous aluminium nitride [which was formed in the perimeter of the insulating layer which consists of at least one sort of highly thermally-conductive materials chosen from aluminium nitride, boron nitride, boron carbide, and diamond-like carbon, the wiring section embedded at said insulating layer, and said wiring section], amorphous silicon nitride, and oxidation silicon, and borosilicate glass.

[0008] Next, the sectional view which expanded drawing 1 and its part for the sectional view of the circuit board concerning this invention is shown in drawing 2, and it explains below at a detail.

[0009] The circuit board 1 is equipped with the base material 2 which consists of at least one sort of highly thermally-conductive materials chosen from aluminium nitride, boron nitride, boron carbide, diamond-like carbon, and a diamond. Two or more laminatings of the insulating layer 3 which consists of said highly thermally-conductive material are carried out on said base material 2. The internal wiring layer 41 used as

the wiring section, and 42 -- 4n-1 and 4n Two or more layers are usually formed in said insulating layer 3. The dielectric film 5 which consists of at least one sort of low dielectric constant ingredients chosen from amorphous aluminum nitride and amorphous oxidation silicon, oxidation silicon, and borosilicate glass is said internal wiring layer 41 and 42. -- 4n-1 and 4n It is formed in the perimeter. The surface wiring layer 6 is formed through the dielectric film 7 which consists of said low dielectric constant ingredient on said insulating layer 3. SURUHORU 8 is said internal wiring layers 41 and 42. -- 4n-1 and 4n And it is formed in order to connect between desired wiring layers among said surface wiring layers 6. In addition, a part is removed, said insulating-layer 3 front face is exposed, and, as for said dielectric film 7 on said insulating layer 3, a semiconductor chip 9 is carried in such an exposure.

[0010] Said internal wiring layer 41 and 42 -- 4n-1 and 4n Inside t1 of the thickness of said insulating layer 3 located in between, and 1, i.e., drawing 2 , It is desirable to make it the range of 0.5-15 micrometers for the following reasons. That is, when thickness (t1) of said insulating layer 3 is set to less than 0.5 micrometers, it is said internal wiring layer 41 and 42. -- 4n-1 and 4n It becomes difficult to separate between electrically enough. On the other hand, when the thickness (t1) of said insulating layer 3 exceeds 15 micrometers, there is a possibility of exfoliating from a substrate (for example, said base material 1) with the internal stress. The thickness (t1) of said more desirable insulating layer 3 is 0.9-10 micrometers.

[0011] Said internal wiring layer 41 and 42 -- 4n-1 and 4n t2 in the thickness of said dielectric film 5 to surround, i.e., drawing 2 , It is desirable to make it the range of 0.4-15 micrometers for the following reasons. That is, when thickness (t2) of said dielectric film 5 is set to less than 0.4 micrometers, it is said internal wiring layer 41 and 42. -- 4n-1 and 4n Covering certainly becomes difficult and it becomes difficult to raise signal velocity of propagation. On the other hand, when the thickness (t2) of said dielectric film 5 exceeds 15 micrometers, there is a possibility of the internal stress of said dielectric film 5 becoming large, and exfoliating from said insulating layer 3.

[0012] Said internal wiring layer 41 and 42 -- 4n-1 and 4n And the thing of multilayer structure, such as aluminum, and Ti/Cu or Ti/nickel/Au, etc. can be used for the surface wiring layer 6.

[0013] Although it is desirable to form through the dielectric film 7 which consists of a low dielectric constant ingredient on said insulating layer 3 as for said surface wiring layer 6, when the leading-about die length of said surface wiring layer 6 is short, it may be directly formed on said insulating layer 3 which consists of said highly thermally-conductive material.

[0014] In addition, it is the internal wiring layer 41 SURUHORU 8 does not need to be surrounded with a dielectric film 7, and is [wiring layer] the wiring section especially when the die length of SURUHORU 8 is short although SURUHORU 8 is surrounded with the dielectric film 7 which consists of a low dielectric constant ingredient in the circuit board shown by drawing 1 , and 42. -- 4n-1 and 4n A dielectric film 7 can be formed only in a perimeter.

[0015] Furthermore, the wiring layer by which the circuit board concerning this invention is embedded into an insulating layer 3 may be a monolayer.

[0016] Next, the manufacture approach of the circuit board concerning this invention is explained to a detail with reference to drawing 3 - drawing 6 .

[0017] First, the insulating layer 12 which consists of highly thermally-conductive material same on the base material 11 which consists of a highly thermally-conductive material mentioned above as shown in drawing 3 (A) is deposited by the thin film forming methods, such as a spatter, a CVD method, the ion plating method, and the cluster ion beam method. In addition, in advance of formation of said insulating layer 12, said base material 11 front face may be defecated by the wet cleaning method, a reverse spatter, etc. It continues, and the low dielectric constant ingredient mentioned above by said thin film forming method after forming two or more slots 13 which have desired width of face and the depth by the almost same die length as the internal wiring layer which should remove said insulating layer 12 alternatively with a photo etching technique, and should form it, as shown in drawing 3 (B) is deposited, and a dielectric 14 is embedded in said slot 13 by removing the dielectric film on said insulating layer 12 further. The dielectric film 15 of a cross-section concave which has the same die length as the internal wiring layer which should be formed as it pulls, and it continues, a photo etching technique removes said dielectric film 1 alternatively and it is shown in drawing 3 (C), width of face, and the depth is formed.

[0018] Subsequently, it is the internal wiring layer 161 of the 1st layer in each dielectric film 15 of said cross-section concave by depositing wiring materials, such as aluminum, on the whole surface by said thin film forming method, and removing the wiring material film of said insulating-layer 12 front face. It embeds. By depositing the low dielectric constant ingredient continued and mentioned above by said thin film forming method, and carrying out patterning, as shown in drawing 4 (D), it is said internal wiring layer

161 of the 1st layer. It reaches, a dielectric film 17 is formed on a dielectric film 15, and it is said internal wiring layer 161. A perimeter is covered with the dielectric film 15 and said dielectric film 17 of said cross-section concave. It pulls, and it continues and the insulating layer 18 which consists of a highly thermally-conductive material mentioned above on the whole surface as shown in drawing 4 (E) is deposited by said thin film forming method. Furthermore, as shown in drawing 4 (F), it is said internal wiring layer 161 of the 1st layer. After forming two or more slots 19 which remove alternatively said insulating layer 18 of the upper predetermined location with a photo etching technique, and even said dielectric film 17 attains, the low dielectric constant ingredient mentioned above in said slot 19 is deposited by said thin film forming method, and a dielectric 20 is embedded by removing the dielectric film on said insulating layer 18 in said slot 19.

[0019] Subsequently, as shown in drawing 5 (G), a photo etching technique removes a dielectric 20 alternatively in said slot 19, and it is said internal wiring layer 161. After carrying out opening of the hole which reaches to a top face, a wiring material is deposited by said thin film forming method, and SURUHORU 22 with which it was embedded in the aforementioned hole and the perimeter was covered with the dielectric film 21 is formed by removing the conductor-material film on said insulating layer 18. It continues, as shown in drawing 5 (H), the insulating layer 23 which consists of a highly thermally-conductive material mentioned above on the whole surface is deposited by said thin film forming method, a photo etching technique removes said insulating layer 22 alternatively, and after forming two or more slots 24 which have desired width of face and the depth by the almost same die length as the internal wiring layer which should be attained and formed up to said insulating-layer 18 front face, a dielectric 25 is embedded by the approach same with having mentioned above in said slot 24. It pulls, and as shown in drawing 5 (I), the dielectric film 26 of a cross-section concave which has the same die length as the internal wiring layer which should remove alternatively said dielectric 25 in said slot 24 with a photo etching technique, and should form it, width of face, and the depth is formed, it continues and said dielectric 25 with which said SURUHORU 22 exists further carries out opening of the ** length-like hole which etches using another mask and reaches said SURUHORU 22. Then, it is the internal wiring layer 162 of the 2nd layer by carrying out the volume of the wiring material into the aforementioned hole formed on the dielectric film 26 of said cross-section concave, and said Sai chief SURUHORU 22. It embeds.

[0020] Subsequently, as shown in drawing 6 (J), it is said internal wiring layer 162 of the 2nd layer. After forming by the technique of having mentioned above the dielectric film 28 which consists of a low dielectric constant ingredient mentioned above upwards, the insulating layer 29 which consists of a highly thermally-conductive material mentioned above on the whole surface is deposited by said thin film forming method. It is said internal wiring layer 162 of the 2nd layer by drawing 4 (F) continued and mentioned above and the same approach as the process of drawing 5 (G). Two or more slots 30 which remove alternatively said insulating layer 29 located on an internal wiring layer predetermined [inner] with a photo etching technique, and even said dielectric film 28 attains are formed. A dielectric is embedded in said slot 30, a photo etching technique removes said dielectric alternatively, and it is said internal wiring layer 162 of the 2nd layer. After carrying out opening of the hole which reaches to a top face, SURUHORU 32 with which the perimeter was covered with the dielectric film 31 is formed by embedding a wiring material in the aforementioned hole (drawing 6 (K) illustration).

[0021] Subsequently, the circuit board of the structure shown in drawing 1 which repeated the process of drawing 5 (H) mentioned above, drawing 5 (I), drawing 6 (J), and drawing 6 (K), and was already explained is manufactured. However, formation of SURUHORU for connecting with the internal wiring layer of the maximum upper layer is faced formation and said front wiring of a surface wiring layer. The dielectric film which consists of a low dielectric constant ingredient is deposited on the insulating layer of the maximum upper layer. Slot formation, Perform embedding into the embedding of a dielectric, opening of a hole, and the aforementioned hole of conductor material, and a through hole is formed. After forming a surface wiring layer on said dielectric film furthermore, the insulating layer which removes alternatively said dielectric film which becomes the loading field of a semiconductor chip, and consists of a highly thermally-conductive material under said dielectric film is exposed.

[0022]

[Function] The circuit board concerning this invention has structure possessing the dielectric film which consists of at least one sort of low dielectric constant ingredients chosen from the amorphous alumimium nitride formed in the perimeter of the insulating layer which consists of at least one sort of highly thermally-conductive materials chosen from alumimium nitride, boron nitride, boron carbide, diamond-like carbon, and a diamond as shown in drawing 1 mentioned above, the wiring section embedded at said insulating

layer, and said wiring section, amorphous oxidation silicon, oxidation silicon, and borosilicate glass. For this reason, when semiconductor chips, such as LSI, are carried in the front face of said circuit board, the heat generated from said semiconductor chip can be emitted good by the insulating layer which consists of said highly thermally-conductive material. Moreover, since the perimeter of said wiring section is covered with the dielectric film which consists of said low dielectric constant ingredient, it can raise the signal velocity of propagation of said wiring section. Therefore, the circuit board which combines high-speed operation nature and high heat dissipation nature can be offered.

[0023] Moreover, as mentioned above, it becomes possible to use the dielectric film which consists of an insulating layer which consists of said highly thermally-conductive material by manufacturing the circuit board concerning this invention according to a thin film process, and a low dielectric constant ingredient as a configuration member of the circuit board, and it controls that the wiring material further used for the wiring section is spread in said insulating layer and said dielectric film, and the wiring section of low resistance can be realized.

[0024] That is, according to the conventional ceramic sintering process, when the sintering temperature of the dielectric film which consists of an insulating layer which consists of said highly thermally-conductive material, and said low dielectric constant ingredient differs, it is difficult to make these live together in the same circuit board. For example, when aluminium nitride (AlN) is used as an insulating layer and borosilicate glass is used as a dielectric film, respectively, in the conventional ceramic sintering process, sintering temperature differs from 1700-1900 degrees C and 400-900 degrees C greatly, respectively. For this reason, it is impossible to form by turns the dielectric film which consists of for example, an insulating layer which consists of an AlN sintered compact, and a borosilicate glass ceramic. Moreover, when forming the wiring section of the circuit board with a thick-film technique, in order to raise adhesion reinforcement with an insulating layer, various kinds of additives including an inorganic substance are usually blended with a wiring material. For this reason, the resistivity of the wiring section formed in said circuit board becomes high compared with what consists of a pure metal.

[0025] On the other hand, since the thin film process mentioned above can form the dielectric film which consists of an insulating layer which consists of said highly thermally-conductive material at low temperature compared with said ceramic sintering process, and said low dielectric constant ingredient, it can manufacture the circuit board of this invention which has the high-speed operation nature and high heat dissipation nature of a signal. And the degree of freedom of the combination of the ingredient of said insulating layer and a dielectric film is also raised. Furthermore, since process temperature can be made into low temperature (for example, 480 degrees C or less) while purity can use 99.99% or more of metal as a wiring material, it controls that the wiring material used for the wiring section is spread in said insulating layer and said dielectric film, and the wiring section of low resistance can be realized.

[0026]

[Example] Hereafter, the example of this invention is explained to a detail.

[0027] In the process which manufactures the circuit board shown in drawing 3 mentioned above example 1-7 - drawing 6, it formed on the conditions which show an insulating layer in the following table 1, and the line manufactured the circuit board shown in drawing 1 mentioned above by the conditions which show a dielectric film in the following table 2 on the conditions which show etching at the time of patterning of said insulating layer and a dielectric film in the following table 3, respectively. However, the base material used the same highly thermally-conductive material as said insulating layer, respectively. Moreover, the wiring material used for an internal wiring layer and a surface wiring layer and its thickness were written together to the following table 3.

[0028]

[Table 1]

実施例	絶縁層					
	高熱伝導性材料	成膜方法	基材温度(℃)	真空度(Pa)	成膜速度(nm/min)	厚さ(μm)
1	AlN	スパッタ	100	0.5	20	9
2	AlN	スパッタ	50	1	15	10
3	SiC	CVD	400	50	600	5
4	BN	CVD	250	20	50	3
5	ダイヤモンドライカーボン	CVD	150	50	100	10
6	ダイヤモンド	CVD	300	100	100	5
7	AlN	CVD	480	50	100	3

[0029]

[Table 2]

実施例	誘電体膜					
	低誘電率材料	成膜方法	基材温度(℃)	真空度(Pa)	成膜速度(nm/min)	厚さ(μm)
1	硼珪酸ガラス	スパッタ	50	1	10	7
2	非晶質AlN	スパッタ	-100	0.6	105	8
3	SiO ₂	スパッタ	200	0.8	50	4
4	非晶質SiO ₂	スパッタ	-50	1.1	200	2
5	硼珪酸ガラス	スパッタ	-80	0.2	90	5
6	硼珪酸ガラス	スパッタ	-100	1	150	3
7	SiO ₂	CVD	400	200	100	1

[0030]

[Table 3]

実施例	絶縁層／誘電体膜エッチング条件		配線	
	エッチング方法	エッチャント	配線材料	膜厚(μm)
1	湿式	HF	Al	5
2	湿式	NH ₄ OH	Ti/Ni/Au	5
3	ドライ	BCl ₃	Al	2
4	ドライ	BCl ₃	Al	1
5	湿式／ドライ	HF/O ₂	Al	3
6	湿式／ドライ	BCl ₃ /O ₂	Al	1
7	湿式／ドライ	HF/BCl ₃	Al	0.5

The apparent signal delay per unit length in an insulating layer, and the adhesion reinforcement of a dielectric film, the dielectric constant of the perimeter of an internal wiring layer and an internal wiring layer

and the thermal conductivity of an insulating layer were measured about the circuit board of the acquired examples 1-7. The result is shown in the following table 4. In addition, said adhesion reinforcement puts said each circuit board to two atmospheric pressures and a 121-degree C ambient atmosphere, makes 1 cycle actuation cooled to a room temperature, and measures the condition after 1000 cycles.

[0031]

[Table 4]

実施例	回路基板の評価			
	密着強度 (MPa)	誘電率* (ε)	単位長さ当たりの信号 遅延時間 (ピコ秒/cm)	熱伝導率 (W/m·K)
1	20	6	81.6	150
2	21	6	81.6	200
3	23	3.8	64.9	110
4	25	2.8	55.7	150
5	20	1.5	40.8	2500
6	20	3	57.8	3000
7	21	4	66.6	300

誘電率*は、内部配線層周囲の値を示す。

It turns out that the circuit board of this examples 1-7 has thermal conductivity with early still higher signal velocity of propagation highly [adhesion reinforcement] so that clearly from said table 4. Therefore, when a semiconductor chip was carried like drawing 1 mentioned above in the circuit board of this examples 1-7, while being able to radiate the heat from a semiconductor chip good, since the signal velocity of propagation of an internal wiring layer was raised, it was possible to have carried out high-speed operation of said semiconductor chip.

[0032] Except having not formed a dielectric film in the interior wiring layer of the example of a comparison, and the perimeter of SURUHORU, the same circuit board as an example 1 was manufactured, and each property was measured. Consequently, it was checked that its apparent signal delay is as large as 99.9 picoseconds / cm since [although the heat transfer rate of an insulating layer was good,] its dielectric constant in the insulating layer of the perimeter of an internal wiring layer is as large as 9.0, 150 W/m-K and, and the correspondence to improvement in the speed is difficult for it.

[0033]

[Effect of the Invention] As explained in full detail above, while raising the signal velocity of propagation of the wiring section according to this invention, it has high temperature conductivity and the circuit board which combines high-speed operation nature and high heat dissipation nature can be offered.

[Translation done.]

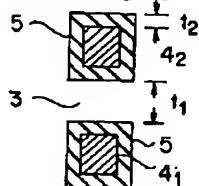
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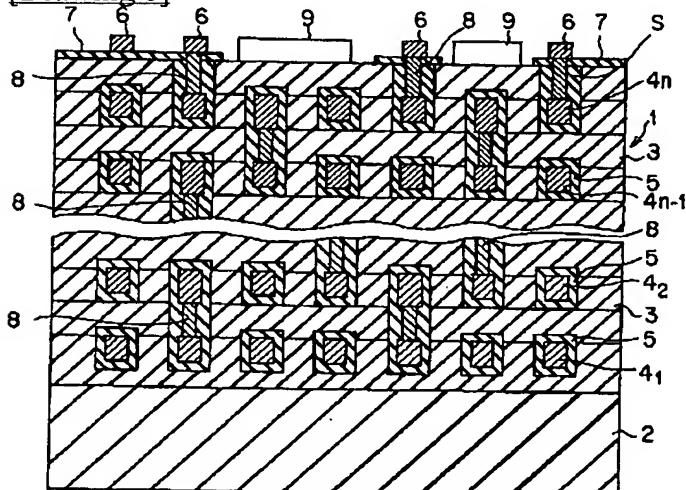
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DRAWINGS

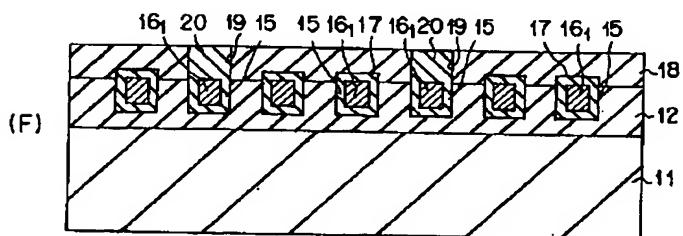
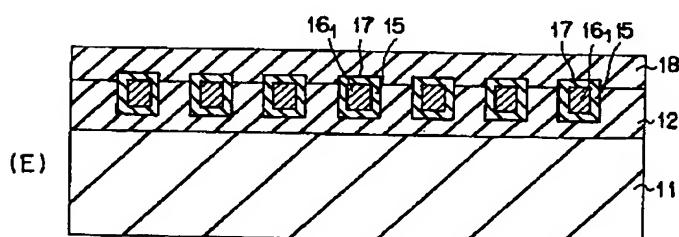
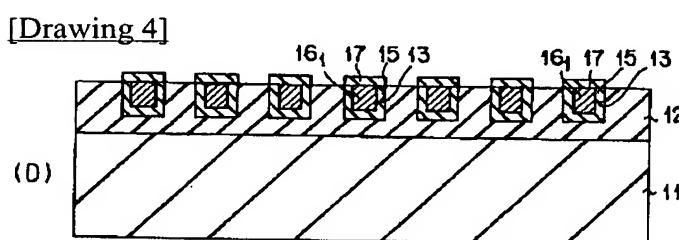
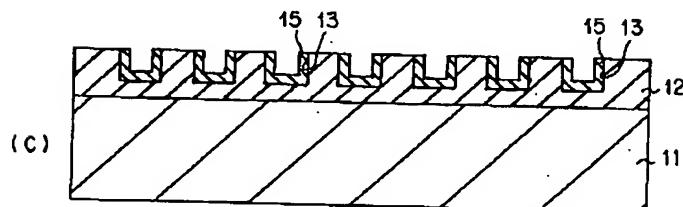
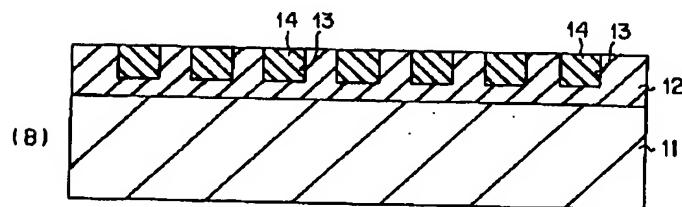
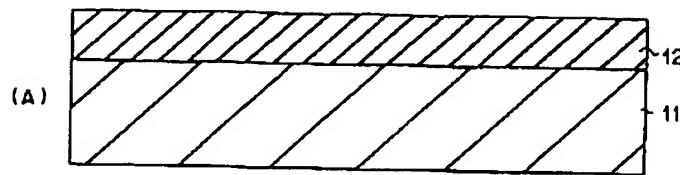
[Drawing 2]



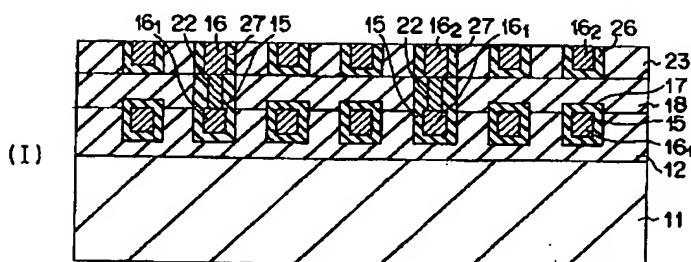
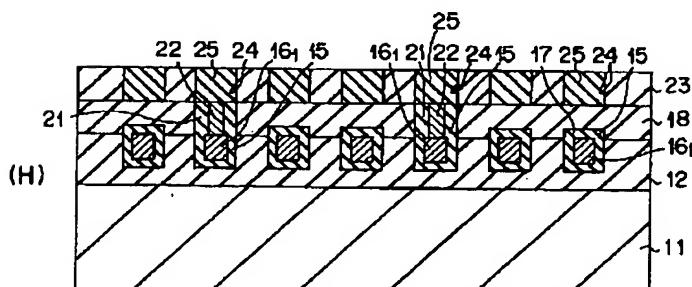
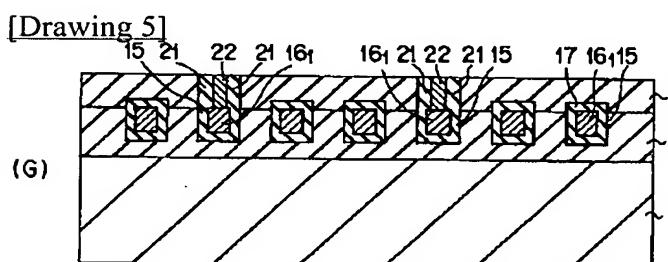
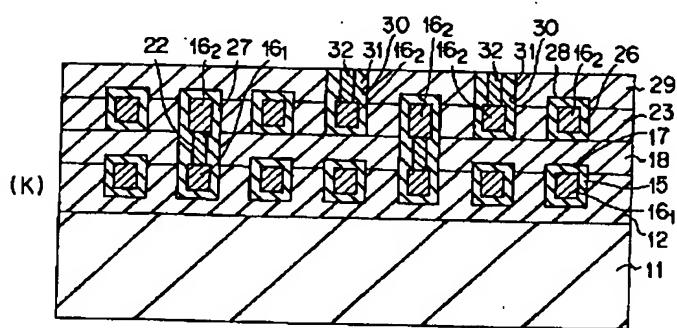
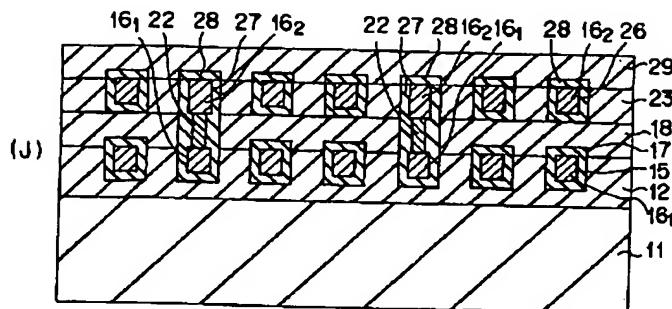
[Drawing 1]



[Drawing 3]



[Drawing 6]



[Translation done.]

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